Remarks

Claims 28, 33, 37, 38, 40, 42, 45, 49, 56, 114, 118 and 129 have been amended, claims 39, 41, 115 and 124-127 have been canceled and new claims 131-137 have been added. Review and reconsideration in light of the amendments and remarks below are respectfully requested.

Claims 21, 31-56 and 113-130 are rejected as being unpatentable over U.S. Pat. No. 6,525,864 to Gee et al. Although the Gee reference is listed on a Form PTO-892 ("Notice of References Cited") in the outstanding Office action, it is noted that the Gee reference was cited by the Applicants in an Information Disclosure Statement mailed on April 30, 2004. The Gee reference was indicated to have been previously considered in the Office action of June 7, 2005.

By way of background, the Gee reference is directed to an entirely different device manufactured in a distinctly different manner than the device of the present invention. More particularly, as can be seen in Fig. 4 of the Gee reference, that device includes a mirror 402 located above metal layers (Metal-3 and Metal-2), which are in turn located above a CMOS layer 421. The CMOS circuitry 421 is located below the mirror 402 and thus the mirror array 410 and CMOS circuitry 421 are directly and fully integrated. A plurality of bond pads 501 (also shown in Fig. 5) are provided such that inputs and outputs can be provided via a wire bond 413 (Fig. 4).

In contrast, in one embodiment the control circuitry of the present invention is not integrated with, or directly coupled to the mirror array, and instead a modular arrangement is provided. For example, as shown in Fig. 8 of this application, the microstructure includes a solderable surface 88 which includes a plurality of pads 80 arranged in a predetermined pattern. The pads 80 are not located under the upper wafer 34 (i.e. are outside the coverage area) and are laterally offset therefrom. The microstructure includes an electronic component, such as a chip 81, which has a plurality of contacts 83 located thereon, and the contacts 83 are arranged in a pattern matching that of the pads 80. In this manner, the electronic component 81 can be inverted and directly attached to the solderable surface 88 such that each contact 83 contacts an associated pad 80. Because each contact 83 is aligned with an associated pad 80, the chip 81 and

solderable surface 88 are directly electrically coupled in a flip chip bonding process, without the need for wire bonds.

Thus, in the system of the present invention, the upper wafer 34 and the electronic component 81 are both coupled to what may be termed a "dummy" lower wafer 66 which may not necessarily include any active electronic components located thereon. This assembly provides a modular nature to the microstructure of the present invention and allows the mirror array (i.e., upper wafer 34) to be fabricated separately from the electronic components 81 (as described at page 10, last line – page 11, line 10 of this application).

This modular manufacturing increases yields since faulty or unacceptable wafer stacks and/or electronic components can be discarded before they are joined. For example, the wafer stack can be tested, before it is coupled to the electronic component, by applying electrical probes and actually operating the mirror array (microstructure). In addition, the modular nature of the invention and ease of access allows an electronic component 81 to be replaced and/or upgraded. In contrast, in the Gee reference provides a completely opposite configuration. The CMOS layer 421 is located below and fully integrated with the mirror array 410. The CMOS layer is not located outside the coverage area and is not joined by flip chip bonding, and does not provide the modular benefits of the present invention.

Accordingly, claim 28 has been amended to specify that the claimed solderable surfaces are arranged in a pattern. Claim 28 has also been amended to include the element of an electronic component that has a plurality of contacts located thereon, wherein the plurality of contacts are arranged in a pattern corresponding to the pattern of the solderable surfaces such that the electronic component is directly mechanically and electrically attachable to the solderable surfaces by a flip chip bonding process.

The Office action has construed the bond pad 501 of the Gee reference as the claimed solderable surface. However, the bond pad 501 of the Gee reference merely provides a location for a wire bond 413 for external connection. The Gee reference does not disclose any "flip-chip" bonding to the bond pad 501, and does not disclose the bond pads 501 being located in a pattern

and an electronic component having a plurality of contacts arranged in a corresponding pattern to allow direct mechanical and electrical attachment as is specified in claim 28.

Furthermore, in order to even further distinguish over the Gee reference, claim 28 has been amended to clarify that the electronic component is directly mechanically and electrically attachable to the solderable surfaces *without the use of wire bonds*. In contrast, the Gee reference only discloses wire bonding to the bond pad 501. Besides not disclosing any flip-chip bonding, the bond pads 501 of Gee do not appear to be configured or designed to accommodate flip-chip bonding. Accordingly, it is submitted that claim 28 patentably distinguishes over the cited references.

Independent claim 56 has been amended to further emphasize the modular nature of the invention. More particularly claim 56 specifies that the microstructure system includes: 1) a lower wafer or wafer portion; 2) an upper wafer or wafer portion including a microstructure, the upper wafer/wafer portion defining a coverage area in top view and being directly coupled to the lower wafer/wafer portion; and 3) an electronic component directly coupled to the lower wafer or wafer portion. Thus, claim 56 specifies that both the upper wafer/wafer portion and the electronic component are directly coupled to the lower wafer/wafer portion. With reference to Fig. 4 of the Gee reference, if the carrier 408 is construed as the lower wafer/wafer portion, it can be seen that the upper wafer/wafer portion 410 is not directly coupled to the lower wafer/wafer portion 408. Instead, the CMOS layer 421 is disposed between the upper wafer/wafer portion 410 and the lower wafer/wafer portion 408.

In addition, claim 56 specifies that the electronic component is generally not positioned under the upper wafer or wafer portion. In contrast, it can seem that the CMOS layer 421 of Gee is almost entirely positioned under the upper wafer/wafer portion 400. Thus, it is submitted that claim 56 patentably distinguishes over the cited references.

It is noted that at page 6, lines 8-9 of the Office action, in the rejection of claim 56, the Office action takes the position that the manufacture of the microsystems is greatly simplified by including an "external" electronic component. This statement is apparently provided to support

an obviousness rejection of claim 56 and appears to acknowledge that the Gee reference lacks the claimed electronic component. However, it is noted that Applicants' application, at page 11 lines 6-10, specifically indicates that the present invention provides "modular" manufacturing that improves the yield of the end product and "improves efficiency of manufacturing."

MPEP §2145 notes that "any judgment on obviousness is in a sense a reconstruction based on hindsight reasoning, but so long as it . . . *does not include knowledge gleaned only from applicant's disclosure*, such a reconstruction is proper." In this case, the Office action uses a benefit ("simplified" manufacture) that is essentially identical to the benefits cited in the application ("improved efficiency" and "modular" manufacturing) to reconstruct applicant's invention. No independent motivation for providing an "external" electronic component is provided in the Office action. In addition, the Gee reference does not appear to recognize any need for use of an "external" electronic component, and does not recognize the benefits of such an arrangement as specified in Applicants' disclosure. Accordingly, it is submitted that, for this additional reason, the claim 56 is patentable over the cited art.

Independent claim 118 specifies that the electronic component is coupled to the solderable surface by flip chip bonding. In contrast, the Gee reference does not disclose flip chip bonding an electronic component to the bond pad 501. Instead, the bond pad 501 is coupled to the carrier by a wire bond 413. In addition, claim 118 has been amended to clarify that the flip chip bonding process does not include wire bonds. Thus, it is submitted that claim 118 patentably distinguishes over the cited references.

Independent claim 129 specifies that the solderable surface is configured to receive an electronic component thereon in a flip chip attachment manner and has been amended to clarify that this flip chip attachment is without wire bonds. In contrast, the bond pad 501 of the Gee reference is configured to be electrically coupled by a wire bond and is not configured to receive an electronic component thereon in a flip chip attachment process.

Applicant has included with this Amendment a web page print out that provides various definitions for the term "flip chip" provided by a Google search. This print out shows that the

claimed flip chip process is distinct from wire bonding. For example, the last definition on the print out is provided by Wikipedia.org and notes that "a flip chip is one type of IC chip mounting which does not require any wire bonds." Thus, it is submitted that the independent claim 129 patentably distinguishes over the cited references.

Although each independent claim is believed to be patentable, the rejection of certain dependent claims are briefly discussed herein.

Claim 34 specifies that the upper wafer and lower wafer portions are coupled together by a photopatternable adhesive. Claim 35 specifies that the photopatternable adhesive is benzocyclobutane, and claim 36 specifies that the upper and lower wafer portions are coupled together by a relatively low activation temperature adhesive having a reflow temperature less than about 125°C. The Office action takes the position it would have been obvious at the time the invention was made to have used the subject matter specified in claims 34-36 to couple together upper and lower wafer portions. However, it is noted that the subject matter of claims 34-36 is the result of engineering skill and development and the bare assertion that it would have been "obvious" to one of ordinary skill in the art is respectfully traversed. For example, compatibility of materials, proper adhesive strength and temperature sensitivity must all be balanced. The Office action has not cited to any art showing the claimed features.

Dependent claim 51 specifies that the upper wafer portion includes a silicon layer, wherein the reflective surfaces are non-silicon material located on the silicon layer. The Office action takes the position that it would have been obvious at the time of the invention to have provided a reflective coating. However, it is noted that when the mirrors are made of silicon, time and cost savings may result in that the base silicon layer can be used as a mirror material, as in the Gee reference, and the time and expense of adding an additional reflective layer is avoided. Further, a method for adhering the reflective coating must be developed, and all materials and processes have to be compatible with each other. Again, no art which discloses this feature is cited in the Office action. Accordingly, it is submitted that claim 51 further distinguishes over the Gee reference.

Claim 53 specifies that the upper wafer portion includes at least a portion of at least one silicon-on-insulator wafer. The Office action takes the position that the Gee reference discloses the subject matter of claim 53. However, this position is respectfully traversed as, for example, Fig. 4 of the Gee reference discloses only a monolithic mirror array 410 and does not appear to disclose any sort of a silicon-on-insulator wafer.

New claim 131 specifies that the electronic component is located generally entirely outside the coverage area. In contrast, the electronic component (i.e., CMOS layer 421) of the Gee reference is not located generally outside of the coverage area of the upper wafer 400. Instead, the CMOS layer 421 is generally located directly below (and therefore inside the coverage area of) the upper wafer 400.

New claim 132 specifies that the upper wafer portion is directly coupled to the lower wafer portion, and the electronics component is directly coupled to the lower wafer portion. In contrast, as described above in the context of claim 56, in the Gee reference the electronics component 421 is positioned between the upper wafer portion 400 and the lower wafer portion 408 and prevents the upper wafer portion 400 from being directly coupled to the lower wafer portion 408.

New claim 133 specifies that the microstructure does not include any active electronics positioned directly below the upper wafer portion that can control, operate or receive inputs from the microstructure. In contrast, in the Gee reference the CMOS layer 421 is positioned directly below the upper wafer portion 400.

New claim 134 is similar to claim 132, but specifies that the electronic component is generally not positioned directly under the upper wafer portion. Finally, new claim 135 depends from 56 and includes limitations similar to those included in claim 28 and discussed above.

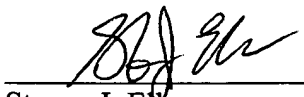
Thus, in sum, it is submitted that the application is in a condition for allowance, and formal notice thereof is respectively solicited.

It is noted that Applicants filed a Supplemental Information Disclosure Statement on April 20, 2006, and consideration of the art cited therein is respectfully requested.

Applicants hereby petition under 37 C.F.R. §1.136 for an extension of time of one month to respond to the outstanding Office Action. The attached check incorporates the $120.00 fee for a response within the first month. (37 C.F.R. §1.17(a)).

The Commissioner is hereby authorized to charge any additional fees required, including the fee for an extension of time, or to credit any overpayment to Deposit Account 20-0809. The applicant(s) hereby authorizes the Commissioner under 37 C.F.R. §1.136(a)(3) to treat any paper that is filed in this application which requires an extension of time as incorporating a request for such an extension.

Respectfully submitted,



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Web

Related phrases: bump or flip chip bonding

Definitions of **flip chip** on the Web:

- A surface mount chip technology where the chip is packaged in place on the board and then underfilled with an epoxy. A common technique for attachment is to place solder balls on the chip, "flip" the chip over onto the board and melt the solder.
  www.xilinx.com/publications/glossary.htm

- another name for a bumped die. Bumped die are flipped over to solder them down, hence the name flip chip.
  www.icknowledge.com/glossary/f.html

- A semiconductor chip that is flipped (face down) and connected for package, substrate or board. The chip typically has bumps (on the bond pads) in a peripheral or array design.
  www.sixsigmaservices.com/glossary.asp

- Unpackaged silicon dies that have been supplied with solder balls directly on the active side of the die. They are called flip chips because they are flipped upside-down, compared to a conventional wirebonded chip.
  www.eppic-faraday.com/glossary.html

- A flip chip is one type of IC chip mounting which does not require any wire bonds. Instead the final wafer processing step deposits solder beads on the chip pads. After cutting the wafer into individual dice, the "flip chip" is then mounted upside down in/on the package and the solder reflowed. Flip chips then normally will undergo an underfill process which will cover the sides of the die, similar to the encapsulation process. ...
  en.wikipedia.org/wiki/Flip_chip

Find definitions of **flip chip** in: **English** French German all languages